memory cells of said peripheral group, so that all peripheries of each memory cell of said internal group are completely surrounded by other memory cells, the number of said internal groups of memory cells being said 2^N or less and a selection circuit coupled to said receiving means and said internal group of memory cells without being connected to said peripheral group of memory cells for selectively accessing only [at least one of] said internal group of memory cells in accordance with said address information.

~~6.~~ (Amended) The memory device according to claim ~~4~~ 1 further comprising at least one dummy word line coupled to a part of said internal group of [dummy] cells and means for operatively activating said dummy word line irrespective of said address information.

Claim 7, line 2, delete "and each of said dummy cells".

(Please add the following new claims.)

~~8~~ 9. A semiconductor memory device comprising an array of memory cells arranged in a matrix form of rows and columns with four peripheries, a plurality of dummy cells arranged along all of said four peripheries of said array, each of said dummy cells having substantially the same configuration as each of said memory cells, address means for receiving address information, and a selection circuit coupled to said address means and said array for selectively accessing at least one memory cell of only

said array of memory cells, all of said dummy cells being not coupled to said selection circuit and not capable of selection by said selection circuit, whereby each of said array of memory cells to be accessed by said selection is completely surrounded by other memory cells of said array or other memory cells of said array and said dummy cells.

~~55~~. The memory device according to claim ~~8~~ 4, in which each of said memory cells and each of said dummy cells includes a floating gate type field effect transistor.

~~56~~. The memory device according to claim ~~8~~ 4, further comprising at least one dummy word line coupled to a part of said dummy cells and means coupled to said dummy word line for operatively activating said at least one dummy word line irrespective of said address information.---

REMARKS

Applicant files concurrently herewith the petition and fee for extension of time pursuant to 37 CFR §1.136. Acknowledgment of receipt and acceptance of the petition and fee are respectfully requested.

The application has been filed with informal drawings acceptable for examination purposes. The drawings have, however, been objected to on form PTO-948. Formal drawings are submitted herewith to replace the informal drawings. Acceptance of the